FACSIMILE TRANSMISSION

TO:

Examiner Luu

USPTO

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FROM:

James H. Ortega

DATE:

June 21, 2002

PAGES:

1 (including this cover page)

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MESSAGE:

Examiner,

Here is the proposed amendment. Analogous changes would be made to independent method claim 7. I believe this distinguishes over the Yamasaki reference because separating Yamasaki's buried conductive regions with a dielectric layer would force the IC chip to be moved to the surface, which would negate the need for the terminals (5) disclosed therein. Please let me know your thoughts. Thank you.

James H. Ortega Reg. No. 50,554

- 1. A process for manufacturing an integrated circuit package comprising:
- (a) forming a substrate having a first dielectric layer, a conductive layer having a first region insulated from a second region and located above the first dielectric layer, and a second dielectric layer above the conductive layer, the second dielectric layer having a cavity wherein the first and second regions are exposed within the cavity and the first region insulated from the second region by a third dielectric layer; and
- (b) interconnecting a first lead of an integrated circuit to the exposed first region and interconnecting a second lead of the integrated circuit to the exposed second region.